



S6LM

IP Camera SoC with Advanced Imaging and Security Features

Overview

Ambarella's S6LM SoC combines state-of-the-art technology with image processing in a single, low-power design. Fabricated using advanced 10 nm process technology, S6LM achieves an industry-leading combination of low-power and high-performance in a wide range of professional and home security IP camera designs.

Meeting the demands of the next generation of intelligent IP cameras, S6LM's architecture provides efficient encoding in both AVC and HEVC video formats capable of up to 5Mp30 + 720p30 + 5Mp1 video. S6LM minimizes cloud storage costs by streaming high-resolution video at low bit rates.

S6LM uses a next-generation image signal processor (ISP) to deliver outstanding imaging in low-light conditions, while its high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes.

S6LM includes a suite of advanced security features to implement advanced on-device physical security, including OTP, TrustZone®, and I/O virtualization.



The S6LM chip targets IP camera designs

Key Features

Advanced Image Processing

- Up to 400 MPixels input rate
- Multi-exposure line-interleaved HDR
- Superior low-light processing
- Hardware dewarping engine
- 3D motion-compensated temporal filtering (MCTF)
- Electronic image stabilization (EIS)
- Up to three independent sensor inputs

High-Efficiency Video Encoding

- H.265 and H.264 video compression
- Flexible multi-streaming capability
- 5Mp30 + 720p30 + 5Mp1 video performance
- Multiple CBR and VBR bit-rate control modes
- Smart H.264 and H.265 encoder algorithms

Flexible Low-Power Platform

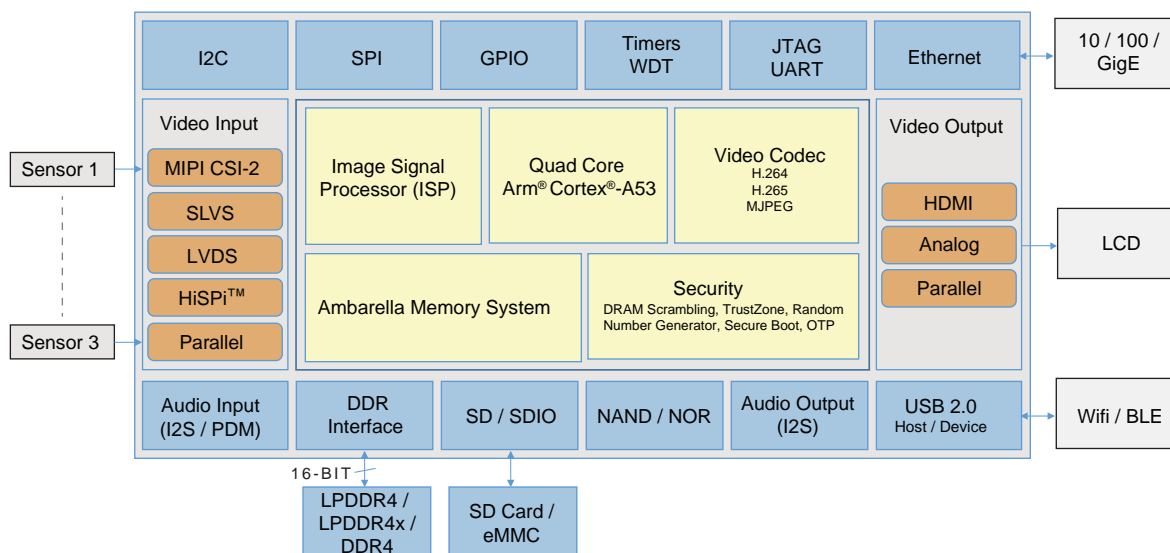
- 64-bit quad-core Arm® Cortex®-A53 CPU up to 1 GHz
- Linux kernel version 4.14 or later (64-bit)
- Linux SDK for standards-based development
- Industry-leading image sensors support
- 10 nm low-power CMOS process

Advanced Cyber-Security Features

- Secure ROM, OTP, and secure boot
- True random number generator
- DRAM scrambling, IO virtualization
- Arm TrustZone

Block Diagram

The diagram below illustrates a design based on the Ambarella S6LM device.



General Specifications

Processor Cores

- Quad-core Arm® Cortex®-A53 up to 1 GHz
- 32KB / 32KB I/D and 1 MB L2 Cache
- NEON™ SIMD and FPU acceleration
- OTP, secure boot, TrustZone®, IO virtualization
- AES / 3DES / SHA-1 / MD5 crypto acceleration
- Ambarella image signal processor and video codec

Sensor and Video I/O

- Single, dual, or triple sensor inputs with independent ISP configuration
- Sub-LVDS / MIPI CSI-2 / SLVS / HiSPi™ input
- 16-bit parallel LVCMOS
- BT.601 / 656 video in and 16-bit BT.601 out
- HDMI® 2.0 including PHY with CEC support
- PAL / NTSC composite SD video out

Sensor Processing

- 400 MPixel/s maximum pixel rate
- Lens shading correction
- Multi-exposure HDR (line-interleaved sensors)
- WDR with local tone mapping

Image Processing

- 3D motion-compensated temporal filtering (MCTF)
- 3-axis electronic image stabilization (EIS)
- Adjustable AE / AWB / AF
- 180° and 360° fisheye lens distortion correction
- High quality polyphase scalars
- Digital PTZ and virtual cameras
- OSD engine, overlays, privacy mask
- Crop, mirror, flip, 90° / 270° rotation
- DC-iris and P-iris
- Defect pixel correction
- Geometric lens distortion correction
- Chromatic aberration correction
- Gamma compensation and color enhancement
- Backlight compensation

Intelligent Video Analytics

- People counting and tracking
- Face detection and recognition
- Human / pet / vehicle classification
- Object classification, recognition, and more
- License plate recognition

Video Encoding

- H.265 MP L5.0, H.264 MP/HP L5.1 and MJPEG
- 5Mp30 + 720p30 + 5Mp1 maximum encoding performance
- Up to 8 simultaneous stream encodes
- Flexible GOP configuration with I, P, and B frames
- Temporal scalable video codec (SVC-T) with 4 layers
- Dynamic region of interest (ROI)
- Multiple CBR and VBR rate control modules

Memory Interfaces

- LPDDR4 / LPDDR4x / DDR4 up to 1.6 GHz, 16-bit data bus
- Three SD controllers: SD / SDIO / SDXC
- Boot from SPI SLC NAND with BCH, SPI NOR, USB, or eMMC

Peripheral Interfaces

- 10 / 100 / 1000 ethernet with RMII / RGMII
- USB 2.0 port configurable for host / device
- Multiple I2S / PDM, SSI / SPI, I2C, and UART
- Multiple GPIO ports, PWM, IR, ADC
- Watchdog timer, multiple general purpose timers, JTAG

Physical

- 10 nm low-power CMOS
- Operating temperature -20°C to +85°C
- FC-TFBGA package with 288 balls, 11x12 mm, 0.65 mm pitch

S6LM IP Camera Development Platform

The S6LM IP Camera Development Platform contains the necessary tools, software, hardware, and documentation to develop an IP Camera utilizing the specialized hardware S6LM provides while supporting development of customized features.

Evaluation Kit (EVK)

- S6LM main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, ON Semi, Omnivision, Panasonic, and others
- Datasheet, BOM, schematics, and layout
- IP Camera reference application with C and C++ source code

Software Development Kit (SDK)

- Linux 4.14 + 64-bit kernel with patches, drivers, tools, and application source code
- Latest Linaro GCC Toolchain for 64-bit ARM Cortex ARM V8
- Royalty-free libraries for ISP, 3A, dewarp, codecs
- Image tuning and manufacturing calibration tools
- Detailed documentation with programmer's guide, application notes

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