



CV2AQ

Automotive Computer Vision SoC

Key Features

Computer Vision Engine **CVflow**[®]

- CNN- / DNN-based monocular processing to enable classification, tracking, and more
- Tools for high- and low-level algorithm development
- CNN toolkit for easy porting with Caffe, TensorFlow, and ONNX

Stereo Processing Engine

- Enabling generic obstacle detection, terrain modeling, and more

High-Efficiency Video Encoding

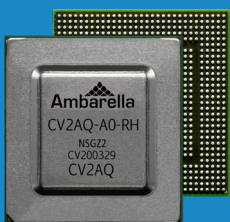
- H.265 and H.264 video compression
- Flexible multi-streaming capability
- 12MP30 video performance
- Multiple CBR and VBR control modes
- Smart H.264 and H.265 encoder algorithms

Ambarella Cutting Edge Imaging Pipeline

- Advanced imaging for low-light conditions
- LED flicker mitigation
- Wide dynamic range (WDR) and high dynamic range (HDR)
- Automotive multi-channel smart auto exposure and auto white balance

Target Applications

- Multi-channel drive recorder
- AVM / surround view with auto parking assist (APA)
- Single- / multi-channel electronic mirror
- Advanced driver-assistance systems (ADAS)
- Driver / in-cabin monitoring system (DMS / CMS)
- Short-range / long-range depth perception camera



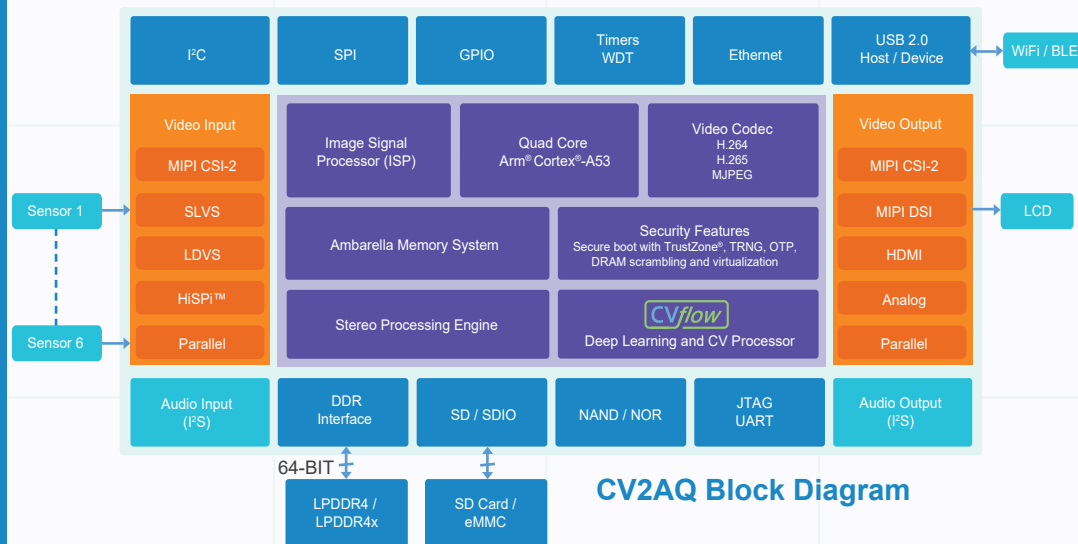
The CV2AQ chip targets automotive sensing camera designs.



Overview

Ambarella's AEC-Q100 qualified CV2AQ SoC combines image processing, 12MP30 video encoding, and CVflow[®] computer vision processing in a single, low-power design. The CV2AQ's CVflow engine's deep neural network (DNN) engine and a dedicated stereo vision accelerator enable efficient implementation of mono and stereo algorithms for the next generation of intelligent automotive cameras. Fabricated in advanced 10 nm process technology, it achieves an industry-leading combination of low-power and high-performance in both human vision and computer vision applications.

The CV2AQ's CVflow architecture provides computer vision processing at full 12MP resolution to enable image recognition over long distances with high accuracy. It includes efficient 4K encoding in both AVC and HEVC video formats, delivering high-resolution video streaming with very low bit rates. The CV2AQ's next-generation image signal processor (ISP) provides outstanding imaging in low-light conditions while high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes, further enhancing the computer vision capabilities of the chip. It includes a suite of advanced cyber-security features such as secure boot with TrustZone[®] and secure memory, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and virtualization, and a programmable secure level for each peripheral interface. A complete set of tools is provided to help customers easily port their own neural networks onto the CV2AQ SoC.



CV2AQ Block Diagram

General Specifications

Processor Cores

- Quad-core Arm® Cortex®-A53 up to 756 MHz
- 32 KB / 32 KB I/D and 1 MB L2 cache
- NEON™ SIMD and FPU acceleration
- Secure boot with TrustZone®, TRNG, OTP, DRAM scrambling and virtualization
- AES / 3DES / SHA-1 / MD5 crypto acceleration

Video Input

- Hexa sensor input with independent ISP configuration
- Sub-LVDS / MIPI CSI-2 / SLVS / HiSPi™
- 16-bit parallel LVCMOS (BT.601 / 656)

Video Output

- 16-bit parallel LVCMOS (BT.601)
- HDMI® 2.0 including PHY with CEC support
- PAL / NTSC composite SD video
- MIPI DSI / CSI-2 and FPD (VESA / JEIDA)

CMOS Sensor / Image Processing


- 12MP30 maximum input resolution
- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)
- 3D motion-compensated temporal filtering (MCTF)
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Adjustable AE / AWB
- LED flicker compensation for LED sources
- Advanced dynamic range (WDR and HDR) engine

- Chromatic aberration correction
- 180° fisheye lens and geometric distortion correction
- OSD engine and overlays
- Gamma compensation and color enhancement
- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, 90° / 270° rotation

Video Encoding

- H.265 MP L5.1, H.264 MP / HP L5.1, and MJPEG
- 12MP30 maximum encoding performance
- Up to 8 simultaneous stream encodes
- Flexible GOP configuration with I, P, and B frames
- Multiple CBR and VBR control modules

Computer Vision Processor

-  processor with parallel architecture to boost performance of the low-level portion of perception algorithms
- Stereo matching
- Feature matching

Tools for Development

- CNN toolkit to ease the porting of CNN trained with Caffe, TensorFlow, or ONNX
- Compiler, debugger, and profiler for both Arm and Microcode development

Memory Interfaces

- LPDDR4x / LPDDR4 up to 1.4 GHz clock rate, 64-bit data bus, up to 4 GB capacity
- Two SD controllers
- Boot from SPI / parallel SLC NAND with BCH / SPI NOR / USB / eMMC
- Single- / dual- / quad-SPI NOR and SPI NAND

Peripheral Interfaces

- One USB 2.0 port configurable as device / host with PHY
- Audio interface including I²S
- Multiple SSI / SPI, IDC, and UART
- Multiple GPIO ports, PWM, Steppers, IR, and ADC
- Watchdog timer, multiple general purpose timers, and JTAG

Physical

- 10 nm low-power CMOS
- HFC BGA package (716 balls, 19x19 mm, 0.65 mm pitch)
- Operating temperature -40°C to + 105°C
- Automotive qualified (AEC-Q100 Grade-2)

CV2AQ Camera Development Platform

The CV2AQ camera development platform contains the necessary tools, software, hardware, and documentation to develop a camera utilizing the powerful CVflow processor while supporting development of customized features.

Evaluation Kit

- CV2AQ main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, ON Semi, Omnivision, and others
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code

Software Development Kit

- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Detailed documentation, including a programmer's guide and more
- CNN / DNN training, profiling, and porting tools

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