CV22S - Computer Vision SoC for IP Cameras

Overview

Ambarella’s CV22S SoC combines image processing, 4Kp30+ video encoding, and CVflow® computer vision processing in a single, low-power design. The CV22S’s CVflow architecture provides the deep neural network (DNN) processing required for the next generation of intelligent IP cameras. Fabricated in advanced 10 nm process technology, it achieves an industry-leading combination of low-power and high-performance in both human vision and computer vision applications.

The CV22S’s CVflow architecture provides computer vision processing at full 4K, to enable image recognition over long distances and with high accuracy. It includes efficient 4K encoding in both AVC and HEVC video formats, delivering high-resolution video streaming with very low bit rates to minimize cloud storage costs. The CV22S’s next-generation image signal processor (ISP) provides outstanding imaging in low-light conditions while high dynamic range (HDR) processing extracts maximum image detail in high contrast scenes, further enhancing the computer vision capabilities of the chip. It includes a suite of advanced security features to implement advanced on-device physical security, including secure boot, TrustZone®, and key storage. A complete set of tools is provided to help customers easily port their own neural networks onto the CV22 SoC.

Key Features

Flexible Low-Power Platform
- 10 nm low-power CMOS process
- 64-bit quad core Arm® Cortex®-A53 CPU up to 1.0 GHz
- Linux kernel version 4.14+ or latest (64-bit)
- CVflow® vector processor with CNN / DNN algorithms
- OTP, secure boot, TrustZone, IO virtualization
- Industry leading image sensors support

Computer Vision Engine
- CNN- / DNN-based processing: detection, classification, tracking, and more
- Computer vision processor
- Tools for high- and low-level algorithm development
- CNN toolkit for easy porting with Caffe, TensorFlow, and ONNX
- Open SDK

Advanced Image Processing
- More than 700 MPixels input rate
- Multi-exposure line-interleaved HDR
- Hardware dewarping engine support
- Electronic image stabilization (EIS)
- Dual independent sensor inputs
- 3D motion-compensated temporal filtering (MCTF)
- Superior low-light processing

High-Efficiency Video Encoding
- H.265 and H.264 video compression
- Flexible multi-streaming capability
- Up to 4Kp30+ video performance
- Multiple CBR and VBR bit rate control modes
- Smart H.264 and H.265 encoder algorithms

Block Diagram

The diagram below illustrates a design based on the Ambarella CV22S device.
CV22S IP Camera Development Platform

The CV22S IP camera development platform contains the necessary tools, software, hardware, and documentation to develop an IP camera utilizing the powerful CVflow processor while supporting development of customized features.

**Evaluation Kit (EVK)**
- CV22S main board with connectors for sensor / lens board and peripherals
- Sensor board: Sony, ON Semi, Omnivision, Panasonic, and others
- Datasheet, BOM, schematics, and layout
- IP camera reference application with C and C++ source code

**Software Development Kit (SDK)**
- Linux 4.14+ 64-bit kernel with patches, drivers, tools, and application source code
- Latest Linaro GCC toolchain for 64-bit Arm Cortex-A53
- Royalty-free libraries for ISP, 3A, dewarp, codecs
- Image tuning and manufacturing calibration tools
- Detailed documentation with programmer’s guide and application notes

**General Specifications**

**Processor Cores**
- Quad-core Arm® Cortex®-A53 up to 1.0 GHz
- 32 KB / 32 KB I/D and 1 MB L2 cache
- NEON™ SIMD and FPU acceleration
- OTP, secure boot, TrustZone
- AES / 3DES / SHA-1 / MD5 crypto acceleration
- Ambarella image and video DSPs

**Sensor and Video I/O**
- Single or dual sensor input with independent ISP configuration
- Single 8-lane sub-LVDS / SLVS / HiSPI™ or dual 4-lane SLVS
- Single 8-lane MIPI or dual 4-lane MIPI CSI-2
- 16-bit parallel LVCMOS
- BT.601 / 656 video in and 16-bit BT.601 out
- HDMI® 2.0 including PHY with CEC support
- PAL / NTSC composite SD video out
- 4-lane MIPI DSI / CSI-2 and FPD (VESA / JEIDA) out

**Front End Sensor Processing**
- More than 700 MPixel/s maximum pixel rate
- Lens shading correction
- Multi-exposure HDR (line-interleaved sensors)
- WDR with local tone mapping

**Image Processing**
- 3D motion-compensated temporal filtering (MCTF)
- 3-axis electronic image stabilization (EIS)
- Adjustable AE / AWB / AF
- 180° and 360° fisheye lens distortion correction
- High quality polyphase scalers
- Digital PTZ and virtual cameras
- OŚD engine, overlays, privacy mask
- Crop, mirror, flip, 90° / 270° rotation
- DC-iris and P-iris
- Defect pixel correction
- Geometric lens distortion correction
- Chromatic aberration correction
- Gamma compensation and color enhancement
- Backlight compensation

**Intelligent Video Analytics**
- CVflow™ vision processor for CNN / DNN edge analytics
- People counting, tracking
- Face detection, tracking, recognition
- Human / pet / vehicle classification
- Object classification, recognition, and more
- License plate recognition

**Video Encoding**
- H.265 (HEVC) MP L5.1, H.264 MP/HP L5.1 and MJPEG
- 4Kp30+ maximum encoding performance
- Up to 8 simultaneous stream encodes
- Flexible GOP configuration with I, P, and B frames
- Temporal scalable video codec (SVC-T) with 4 layers
- Dynamic region of interest (ROI)
- Multiple CBR and VBR rate control modules

**Memory Interfaces**
- LPDDR4 / LPDDR4x up to 1.8 GHz, 32-bit data bus
- Two SD controller with SDXC SD™ card
- Boot from SPI or parallel SLC NAND with BCH, SPI NOR, USB, or eMMC

**Peripheral Interfaces**
- 10 / 100 / 1000 ethernet with RMII / RGMII
- USB ports configurable for host / device
- Multiple I2S, SSI / SPI, I2C, and UART
- Many GPIO ports, PWM, steppers, IR, ADC
- Watchdog timer, multiple general purpose timers, JTAG

**Physical**
- 10 nm low-power CMOS
- Operating temperature -20°C to +85°C
- FBGA package with 441 balls, 14x14 mm, 0.65 mm pitch