Ambarella
AI envisioned

PRODUCT BRIEF

CV3 Family

AI Domain Controller for ADAS and L2+ to L4 Autonomy

Key Features

Computer Vision AI Engine CVflow®
- NN based processing to enable detection, classification, tracking, and more
- NVP with up to 500 eTOPS AI compute and industry-leading power efficiency
- GVP for offloading classical computer vision and radar processing, and floating-point intensive algorithms

Advanced Image Processing
- Multi-exposure, line-interleaved HDR
- Real time multi-scale / multi-FOV generation
- Hardware dewarping engine support
- Multiple camera support
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor

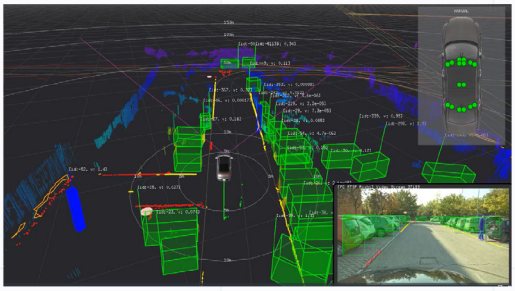
Dense Stereo and Optical Flow Engine
- Generic obstacle detection, terrain modeling, and more

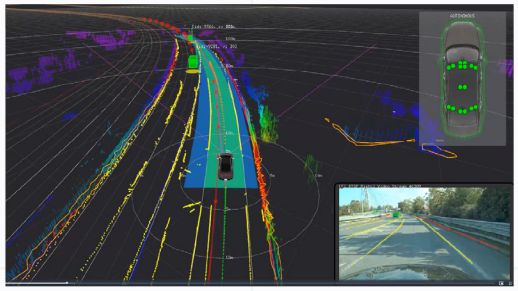
Graphics Processing Unit (GPU)
- Automotive GPU for 3D surround-view rendering

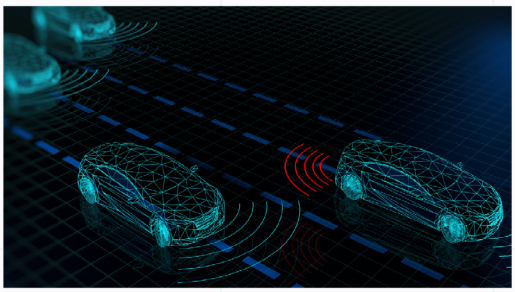
High-Efficiency Video Encoding
- H.265, H.264, MJPEG video encoding
- Flexible multi-streaming capability

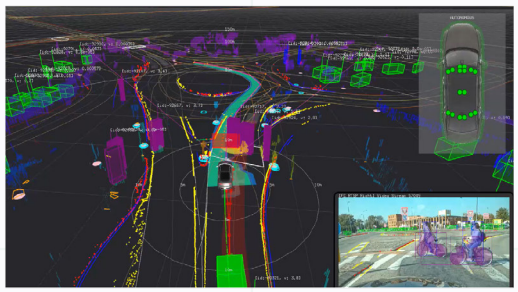
Functional Safety
- Processing island targeted to meet ASIL B requirements; safety island targeted to meet ASIL D requirements
- Error correcting code (ECC) protection of DRAM
- Central error handling unit (CEHU)

Target Applications
- Automated driving from L2+ to L4
- Single- / multi-camera advanced driver assistance systems (ADAS)
- Parking assistance systems
- Driver monitoring systems (DMS) and in-cabin solutions
- Single- / multi-channel electronic mirrors with blind spot detection (BSD)







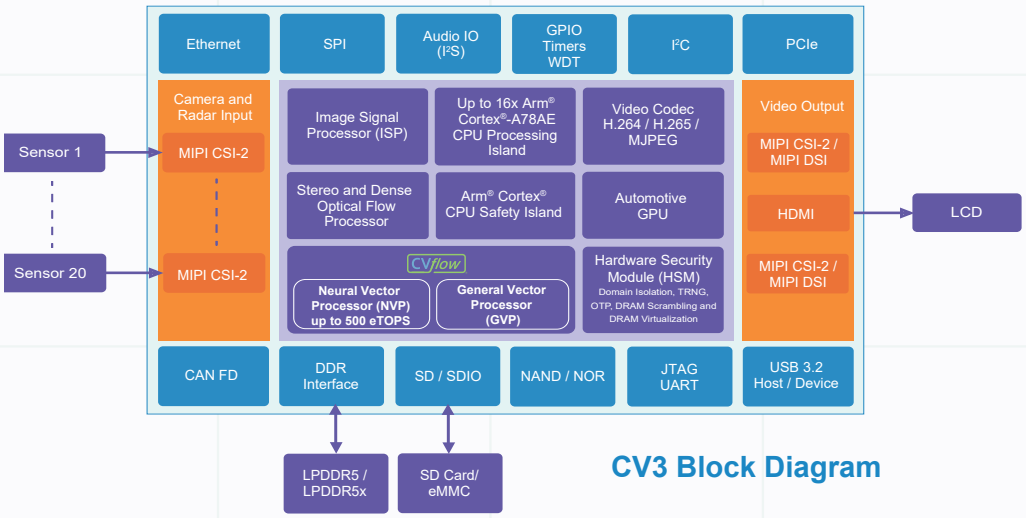


Overview

Ambarella's ASIL B(D)-compliant CV3 domain controller system on chip (SoC) provides up to 500 eTOPS of CVflow AI processing for neural network (NN) computation. In addition, CV3 includes a general vector processor (GVP), an advanced image processor, a dense stereo and optical flow engine, up to 16 Arm® Cortex®-A78AE CPUs, and an automotive GPU, in a single SoC. Ambarella's highly-efficient CVflow®, artificial intelligence (AI) engine enables high performance, low latency, and low-power neural network processing for ADAS and L2+ to L4 autonomous vehicles. The CVflow's neural vector processor (NVP) is enhanced to support the latest advancements in NN inference and offers 42x improvement over Ambarella's existing automotive family of SoCs. The NVP is complemented by the new floating-point GVP, designed to offload classical computer vision and radar processing off the NVP engines and floating-point intensive algorithms from the Arm CPUs.

The ISP provides outstanding imaging in low-light conditions, while its high dynamic range (HDR) processing extracts maximum image detail in high-contrast scenes, enhancing the AI and computer vision capabilities of the chip while delivering crisp video for viewing. CV3 delivers high-resolution video recording and streaming at very low bit rates with efficient encoding in H.265 and H.264 video formats. It includes a hardware security module (HSM), which provides isolation of different domains, secure software provisioning, a suite of advanced cybersecurity features such as asymmetric / symmetric crypto acceleration, secure storage and key provisioning, encrypted CVflow tasks, true random number generator (TRNG), one-time programmable memory (OTP), DRAM scrambling and DRAM virtualization.

Fabricated in an advanced 5 nm process technology, the CV3 is an ideal platform for implementing autonomous driving for vehicles from L2+ to L4, single- and multi-camera ADAS, DMS and in-cabin solutions, single- and multi-channel electronic mirrors with BSD, and intelligent parking assistance systems.



CV3 Block Diagram

General Specifications

Computer Vision AI Processor
- CVflow processor optimized for high-performance and power-efficient, neural network compute
- Neural vector processor (NVP) with up to 500 eTOPS AI compute and industry-leading power efficiency
- General vector processor (GVP) for offloading classical computer vision and radar processing, and floating-point intensive algorithms
- Stereo engine for disparity map generation
- Dense optical flow engine

Processor Cores
- Up to 16 core Arm® Cortex®-A78AE for processing island
- Arm Cortex lockstep cores for safety island
- NEON™ SIMD and FPU acceleration
- AES / SHA1 / SHA2-256 crypto acceleration using Armv8 extensions

Graphics Processing Unit
- Automotive GPU for 3D surround view rendering

Camera and Radar Input
- 12x MIPI CSI-2 (4x-lane, MIPI D-PHY)
- Up to 20 cameras using MIPI virtual channels

Video Output
- HDMI® 2.0 including PHY with CEC support
- Two MIPI CSI-2 / MIPI DSI ports

CMOS Sensor / Image Processing
- Lens shading, fixed-pattern noise correction
- Multi-exposure HDR (line-interleaved sensors)
- 3D motion-compensated temporal filtering (MCTF)
- RGGB / RCCB / RCCC / RGB-IR / monochrome sensor support
- Multi-ROI HW scaler
- Adjustable AE / AWB
- Dynamic range (WDR and HDR) engine
- Chromatic aberration correction
- Geometric distortion correction
- Gamma compensation and color enhancement
- Vignetting compensation
- 3-axis electronic image stabilization (EIS)
- Crop, mirror, flip, 90° / 270° rotation

Video Encoding
- H.264 / H.265 MP / HP L5.0 and MJPEG
- Flexible GOP configuration with I and P frames
- Multiple CBR and VBR rate control modules

Hardware Security Module (HSM)
- Asymmetric / symmetric crypto acceleration, domain isolation, secure storage and key provisioning, encrypted CVflow tasks, TRNG, OTP, DRAM scrambling, and DRAM virtualization

Tools for Development
- Neural Network toolkit to ease the porting of NNs trained using frameworks such as Caffe, TVM, PyTorch, TensorFlow, TensorFlowLite, Keras, and ONNX
- Compiler, debugger, and profiler for both Arm and microcode development

Memory Interfaces
- LPDDR5 / LPDDR5x, up to 256-bit data bus for data, up to 128 GB capacity
- Multiple SD controllers
- Boot from PCIe / SPI NAND / SPI NOR / USB / eMMC
- Single- / dual- / quad- / octal-SPI NOR and single- / dual- / quad-SPI NAND

Peripheral Interfaces
- Multiple 10 / 100 / 1000 Ethernet with RMII / RGMII
- Multiple 4-lane PCIe interfaces
- USB 3.2 host / device and USB 2.0 device only with PHY
- I²S input and output interfaces, DMIC
- Multiple CAN FD interfaces
- Multiplexed UART and I/F of SSI / IDC
- Multiple GPIO ports, PWM, and IR interfaces
- Watchdog timer, general purpose timers, and JTAG

Physical
- 5 nm low-power CMOS
- HFC BGA package
- Operating temperature -40°C to +125°C (T_J)
- Automotive qualified (AEC-Q100 Grade-2, ASIL B(D)

CV3 Domain Controller Development Platform

The CV3 domain controller development platform contains the necessary tools, software, hardware, and documentation to develop ADAS and L2+ to L4 autonomous vehicles utilizing the powerful CVflow processor, while supporting development of customized features.

Evaluation Kit (EVK)
- CV3 main board with connectors for sensor / lens board and peripherals
- Sensor boards
- Datasheet, BOM, schematics, and layout
- SDK and reference application with C source code

Software Development Kit (SDK)
- SDK, OS, and middleware
- Royalty-free libraries for ISP, dewarp, and video recording
- Image tuning and manufacturing calibration tools
- Detailed documentation with programmer's guide and application notes
- Tools to optimize, port, and profile NN / DNN

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